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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

BARAN, MARY C

ART UNIT

PAPER NUMBER

2857

DATE MAILED: 01/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/863,178

Applicant(s)

ORGAN ET AL.

Examiner

Mary Kate B Baran

Art Unit

2857

AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. The action is responsive to the Amendment filed on 29 September 2003. Claims 1-11 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5, and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neisch et al. (U.S. Patent No. 6,269,319) in view of Zwan et al. (U.S. Patent No. 6,098,028) (hereinafter Zwan).

Referring to claim 1, Neisch discloses a method of sequentially connecting one or more testing devices to I/O ports of a DUT through a network, so as to execute a predetermined testing procedure associated with the DUT (see Neisch, column 3 lines 17-26), comprising: receiving one or more commands, wherein each of the commands uniquely specifies an electrical path connecting a particular testing device to a particular I/O port of the DUT (see Neisch, column 4 line 67 – column 5 line 2); and, sequentially implementing the electrical paths corresponding to the one or more commands in a predetermined order (see Neisch, column 5 lines 15-19). Neisch does not teach a network map defining one or more connections within the switching network necessary

to implement each of a plurality of electrical paths from an input of the network to an output of the network, wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT; or for each of the one or more commands, comparing the command to the network map so as to identify a corresponding electrical path through the network, and implementing the corresponding electrical path associated with the command through the network.

Zwan teaches a network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the network to an output of the network (see Zwan, column 5 lines 21-36), wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT (see Zwan, column 5 lines 10-20); or for each of the one or more commands, comparing the command to the network map so as to identify a corresponding electrical path through the network, and implementing the corresponding electrical path associated with the command through the network (see Zwan, column 7 line 47 – column 8 line 8).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Neisch to include the teachings of Zwan because having a switching network map which defines and identifies the various electrical paths would have allowed the skilled artisan to see and point to desired signal paths (see Zwan, column 8 lines 4-8).

Referring to claim 2, Neisch teaches assigning a unique path name to each of the electrical paths, such that each command specifies a particular electrical path via the path name (see Neisch, column 5 lines 2-10).

Referring to claim 3, Neisch discloses implementing the electrical paths associated with the one or more commands through the network in an order corresponding to a chronological order of the one or more commands (see Neisch, column 5 lines 15-17).

Referring to claim 5, Neisch teaches programming a computer system to issue the commands in the predetermined order (see Neisch, column 5 lines 15-17).

Referring to claim 7, Neisch discloses associating each of the electrical paths with a name that is (i) descriptive of the path and (ii) related to the DUT (see Neisch, column 5 lines 2-10).

Referring to claim 8, Neisch teaches a method of sequentially connecting one or more testing devices to I/O ports of a DUT through a network, so as to execute a predetermined testing procedure associated with the DUT (see Neisch, column 3 lines 17-26), comprising: a controller for receiving one or more commands, wherein each of the commands uniquely specifies an electrical path connecting a particular testing device to a particular I/O port of the DUT (see Neisch, column 4 line 67 – column 5 line

2); and sequentially implementing the electrical paths corresponding to the one or more commands in a predetermined order (see Neisch, column 5 lines 15-19). Neisch does not teach a network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the network to an output of the network, wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT; or for each of the one or more commands, comparing the command to the network map so as to identify a corresponding electrical path through the network, and implementing the corresponding electrical path associated with the command through the network.

Zwan teaches a network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the network to an output of the network (see Zwan, column 5 lines 21-36), wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT (see Zwan, column 5 lines 10-20); or for each of the one or more commands, comparing the command to the network map so as to identify a corresponding electrical path through the network, and implementing the corresponding electrical path associated with the command through the network (see Zwan, column 7 line 47 – column 8 line 8).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Neisch to include the teachings of Zwan because having a switching network map which defines and identifies the various electrical paths would

have allowed the skilled artisan to see and point to desired signal paths (see Zwan, column 8 lines 4-8).

Referring to claim 9, Neisch discloses that the network includes at least two sub-networks electrically coupled so as to form the plurality of electrical paths (see Neisch, column 5 lines 26-51 and Figure 3).

Referring to claim 10, Neisch teaches that sub-networks include an SCM (see Neisch, column 3 lines 47-48, i.e. software configuration storage element 91) and a DUT board (see Neisch, column 3 lines 43-47, i.e. Interface Test Adapter 23).

Referring to claim 11, Neisch discloses that each of said one or more commands includes a pin name that is (i) descriptive of the path and (ii) related to the DUT (see Neisch, column 5 lines 2-10).

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Neisch et al. (U.S. Patent No. 6,269,319) (hereinafter Neisch) and Zwan et al. (U.S. Patent No. 6,098,028) (hereinafter Zwan) in view of Yang (U.S. Patent No. 6,098,027).

Referring to claim 4, Neisch and Zwan teach all the features of the claimed invention except for opening and closing selected switching devices within the switching network.

Yang discloses opening and closing selected switching devices within the switching network (see Yang, column 3 lines 47-52 and Figure 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Neisch and Zwan to include the teachings of Yang, because opening and closing switches to select a signal path improves test time and accuracy (see Yang, column 2 lines 28-37).

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Neisch et al. (U.S. Patent No. 6,269,319) (hereinafter Neisch) and Zwan et al. (U.S. Patent No. 6,098,028) (hereinafter Zwan) in view of Mogi et al. (U.S. Patent No. 4,810,958) (hereinafter Mogi).

Referring to claim 6, Neisch and Zwan teach all the features of the claimed invention except for connecting one or more testing devices to multiple DUT sites via the switching network.

Mogi et al. teaches connecting one or more testing devices to multiple DUT sites via the switching network (see Mogi et al., column 2 line 62 – column 3 line 15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Neisch and Zwan to include the teachings of Mogi et al., because testing multiple devices with one switching network allows the skilled artisan to centralize and standardize tests in order to achieve an integrated testing system (see Mogi et al., column 2 lines 19-24).

Response to Arguments

5. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Neisch does not teach a switching network. While Neisch does not specifically teach a switching network map, mapping various electrical paths is disclosed. Further, the Examiner now uses Zwan, who does disclose a network map defining one or more connections within the switching network necessary to implement each of a plurality of electrical paths from an input of the network to an output of the network (see Zwan, column 5 lines 21-36), wherein each of the plurality of electrical paths is representative of a connection of one of the testing devices to one of the I/O ports of the DUT (see Zwan, column 5 lines 10-20); or for each of the one or more commands, comparing the command to the network map so as to identify a corresponding electrical path through the network, and implementing the corresponding electrical path associated with the command through the network (see Zwan, column 7 line 47 – column 8 line 8). It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Neisch to include the teachings of Zwan because having a switching network map which defines and identifies the various electrical paths would have allowed the skilled artisan to see and point to desired signal paths (see Zwan, column 8 lines 4-8).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

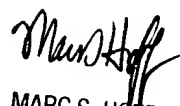
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B Baran whose telephone number is (703) 305-4474. The examiner can normally be reached on Monday - Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (703) 308-1677. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Art Unit: 2857

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

MKB


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800